REMARKS

Reconsideration and allowance of the present application based on the following remarks are respectfully requested.

Upon entry of this Amendment, claims 1, 3, 5, 6, 9 will be pending in this application. Claims 1, 3 and 5 have been amended solely for further clarifying the claim language.

Entry of the Amendment is proper under 37 C.F.R. § 1.116 as the amendments: (a) place the application in condition for allowance for the reasons discussed herein; (b) do not raise any new issues that would require further consideration and/or search as the amendments merely amplify issues discussed throughout the prosecution; (c) do not present any additional claims without cancelling a corresponding number of claims; and (d) place the application in better form for appeal, should an appeal be necessary. The amendments are necessary and were not earlier presented as they are in response to arguments raised in the final rejection. Entry of the Amendment is respectfully requested.

Claim Rejection – 35 USC § 102 and 35 USC § 103

Claims 1 and 5 were rejected under 35 U.S.C. 102(b) over Okonogi (US Pat. No. 5,420,064). The Applicants respectfully traverse this rejection for at least the following reasons.

Claim 1 recites a structure of a dielectrically separated silicon wafer having a plurality of single crystal silicon islands, each of which comprises a high concentration impurity doped flat bottom layer formed on the bottom and a low concentration impurity doped flat upper layer formed on said flat bottom layer constituting the surface layer. This structure is formed by first forming a flat high concentration impurity layer by a diffusion process of a high concentration impurity on the mirror finished surface of a single crystal silicon wafer and forming the upper layer on top of the high concentration impurity layer wherein the upper layer is doped with a low concentration impurity. Accordingly, when a dielectrically separated single crystal wafer is produced by a series of production processes, each single crystal island formed on the wafer has a flat high impurity concentration layer at the bottom and the high concentration impurity layer is entirely covered by the low impurity concentration layer formed on the upper layer.

In contrast, the dielectrically separated wafer obtained by Okonogi's method is formed such that the single crystal silicon islands 11a are separated by polysilicon layer 14, silicon oxide layer 13 and n+ doped layer 12. Specifically, the n+ doped layer 12 is formed

such that it covers the entire bottom surface of each silicon island and as clearly shown in figure 2 of Okonogi, the n+ doped layer 12 is exposed at the periphery of each silicon island 11a (i.e., on the top of the "Λ" shape). Therefore, in order to avoid the diffusion of the n+ doped layer 12, the semiconductor device cannot be formed on the entire surface area of the silicon island because the n+ doped layer 12 is exposed at the peripheral portion of the silicon islands. Consequently, the area available for fabrication of the semiconductor device becomes small.

The present invention, as recited in claim 1, solves this problem since the high concentration impurity layer is not exposed to the surface at a periphery of each single crystal silicon island. Thus, the entire surface of the silicon island can be used for constituting a semiconductor device which allows the usable surface area to be extended to the peripheral regions of the silicon islands. Consequently, Okonogi does not disclose or suggest the structure recited in claim 1.

Therefore, the Applicants respectfully submit that claim 1 is patentable and request that the §102 rejection be withdrawn.

With regard to claim 5, Okonogi does not disclose or suggest that "A dielectrically separated wafer, having a plurality of dielectrically separated monocrystalline silicon islands separated by a dielectrically separating oxide film on the wafer surface, the dielectrically separated wafer comprises a surface between one dielectrically separated silicon island and another neighboring dielectrically separated silicon island formed so as to be flat by controlling the separation polishing of monocrystalline silicon and the dielectric layer." In Okonogi the oxide layer 13, i.e., dielectrically separating layer, is not flat. To the contrary, the dielectric layer in Okonogi is "Λ-shaped", i.e., "pointed", as clearly illustrated in Figures 2, 1E and 3E. Moreover, as shown in Figure 2 in Okonogi, the separation polishing between the monocrystaline silicon 11a and the dielectric layer 13 is maintained constant and therefore is not controlled. Okonogi, in Figure 3D, shows the degree of polishing (see, line 10b) only layers 11 and 12 are polished to a flat surface at the tip of layer 13. Consequently, Okonogi does not disclose or suggest that a surface between to neighboring islands is formed to be flat by "controlling the separation polishing of monocrystaline silicon and the dielectric layer." Therefore, the Applicants respectfully submit that claim 5 is patentable and request that the §102 rejection be withdrawn.

Claims 3, 6 and 9 were rejected under 35 U.S.C. 102(b), or in the alternative, under 35 U.S.C. 103(a) over Okonogi. The Applicants respectfully traverse these rejections for at least the following reasons.

Claim 3 recites, *inter alia*, "said polysilicon layer is formed by a seed low temperature CVD polysilicon layer grown by a low temperature CVD method on the interface with said dielectrically separating oxide film and the polysilicon layer formed by a high temperature CVD method."

The Examiner contends that the limitations that the polysilicon layer has a seed layer grown by low temperature CVD and a polysilicon layer grown by high temperature CVD are considered processing limitations...and are considered merely an obvious processing variant over that taught by Okonogi. The Applicant respectfully submit that process of forming a seed low temperature CVD polycrystalline layer on the dielectrically separating film by a low temperature CVD process and growing a polycrystalline silicon film by a high temperature CVD process is not anticipated or obvious over Okonogi and contrary to the Examiner's contention, is not "a merely obvious processing variant over that taught by Okonogi". Indeed, the formation of a seed low temperature CVD polysilicon film between the dielectrically separating oxide film and the high temperature CVD polysilicon film is a novel process that is very effective in eliminating generation of protrusions or blisters which grow by including particles or protrusions in the oxide layer. Furthermore, if the high temperature CVD polysilicon layer were to be formed directly on the oxide film, the oxide film would be corroded and would lead to formation of pinholes in the oxide film. Consequently, as claimed in claim 3 of the present invention, insertion of the low temperature CVD seed film between the oxide film and the high temperature CVD polysilicon film is indispensable and very effective in producing high-quality dielectrically separated monocrystalline silicon wafers.

Accordingly, Okonogi does not disclose or suggest a polysilicon layer comprised of a low temperature layer and a high temperature layer much less the structure formed. Therefore, the Applicants respectfully submit that claim 3 is patentable and request that the §102 and the §103 rejections be withdrawn.

Claim 6 is dependent upon allowable claim 1. Therefore claim 6 is also allowable for at least the raison that it depends upon allowable claim 1. Claim 9 is dependent upon allowable claim 3. Therefore, claim 9 is also allowable for at least the reason that it depends

upon allowable claim 3. Therefore, the Applicants respectfully submit that claims 6 and 9 are patentable and request that the §102 and the §103 rejections be withdrawn.

CONCLUSION

In view of the foregoing, the claims are now in form for allowance, and such action is hereby solicited. If any points remain in issue which the Examiner feels may be best resolved through a personal or telephone interview, he is kindly requested to contact the undersigned at the telephone number listed below.

Attached is a marked-up version of the changes made to the specification and claims by the current amendment. The attached Appendix is captioned **"Version with markings to show changes made"**.

All objections and rejections having been addressed, it is respectfully submitted that the present application is in a condition for allowance and a Notice to that effect is earnestly solicited.

Respectfully submitted,

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Attached: Appendix

APPENDIX: VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS

The claims were amended as follows:

1. (Twice Amended) A dielectrically separated wafer having a plurality of dielectrically separated monocrystalline silicon islands mutually defined by a dielectrically separating oxide film on a surface of the wafer, wherein said dielectrically separated silicon islands comprise:

a high concentration impurity layer formed on a bottom of the islands in a flat plate form; and

a low concentration impurity layer having an identical conductivity laminated on the plate of the high concentration impurity layer.

3. (Twice Amended) A dielectrically separated wafer having a polysilicon layer and a plurality of monocrystalline silicon islands mutually separated by a dielectrically separating layer consisting of a silicon oxide film which is formed on a surface of a polysilicon layer, wherein:

said polysilicon layer is formed by a seed low temperature CVD polysilicon layer grown by a low temperature CVD method on an interface with said dielectrically separating oxide film and a polysilicon layer formed by a high temperature CVD method.

5. (Twice Amended) A dielectrically separated wafer, having a plurality of dielectrically separated monocrystalline silicon islands [insulated] separated by a dielectrically separating oxide film on the wafer surface, the dielectrically separated wafer comprises a surface between one dielectrically separated silicon island and another neighboring dielectrically separated silicon island formed so as to be flat by controlling the separation polishing of monocrystalline silicon and the dielectric layer.

End of Appendix